UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,331	01/30/2004	Eric R. Keller	X-1557-4 US	7399

24309 7590 05/19/2006

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,331	KELLER ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	TT

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/27/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 01/30/2004. Claims 1-24 are pending.

Specification

1. The disclosure is objected to because of the following informalities: on page 51, the invention title is included in the abstract.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 17, 24, and their dependencies (claims 2-16 and 18-23) are rejected under 35 U.S.C. 112, second paragraph, because the recited " threads" in claims 1, 17, and 24 is not clearly defined in the claims.

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-5, 8-9, 11, 13-21, and 24** are rejected under 35 U.S.C. 102(b) as being anticipated by Davis et al. (US Patent No. 6,230,307).

Referring to claim 1, Davis et al. disclose a method of programming a design tool to implement a message processing system using an integrated circuit, the method comprising:

defining first attributes for a plurality of threads (hardware objects) within said integrated circuit (Davis et al. , col. 3, lines 25-30 see "hardware objects; Fig. 9-10, col. 8, line 39 to col. 9, line 38);

defining second attributes for a memory associated with said integrated circuit (col. 3, lines 25-30 ; col.9, lines 17-24);

defining third attributes for an interconnection topology associated with at least one of said memory and said plurality of threads (col. 3, lines 25-30 ; col. 17, lines 1-9, see " a direct connection"; col. 9, lines 17-24, see "thread" and "hardware object"); and

defining fourth attributes for an interface to at least one of said memory and said plurality of threads (col. 3, lines 25-30 ; Fig. 5 (element 425), col. 6, lines 46-54; col. 7, lines 16-29 see "the interfaces of the hardware objects").

Claim 2, Davis et al. disclose the method of claim 1, wherein each of said first, second, third, and fourth attributes comprises at least one of functional

attributes and architectural attributes (col.8, lines 39-44; col. 9, lines 17-24; col. 17, lines 1-9; col. 7, lines 16-29).

Claim 3, Davis et al. disclose the method of claim 1, wherein each of said first, second, third, and fourth attributes is defined using a set of primitives (Fig. 6, col. col. 6, lines 55-67).

Claim 4, Davis et al. disclose the method of claim 3, wherein said primitives comprise program code for driving said design tool (Figs. 14 and 21-24; col. 9, lines 5-16; col. 16, line 55 to col. 17, line 17).

Claim 5, Davis et al. disclose the method of claim 4, wherein said program code is callable by a second design tool (col. 9, lines 39-53; col. 3, lines 25-31).

Claim 8, Davis et al. disclose the method of claim 1, wherein said step of defining said first attributes comprises:

specifying an instruction set for each of said plurality of threads (Figs 11-13, col. 9, line 54 to col. 10, line 16; Fig. 16, col. 11, line 21 to col. 12, line 14).

Claim 9, Davis et al. disclose the method of claim 8, wherein said instruction set is configured to define inter-thread communication amongst said plurality of threads (Figs 11-13; col. 9, line 25 to col. 10, line 16; Fig. 16, col. 11, line 21 to col. 12, line 14).

Claim 11, Davis et al. disclose the method of claim 1, wherein said integrated circuit is a programmable logic device (Fig. 1, col. 4, lines 51-58; Fig. 5), and wherein said plurality of threads is implemented (col. 10, lines 30-40) within programmable logic of said programmable logic device (col. 13, lines 16-24).

Claim 13, Davis et al. disclose the method of claim 11, wherein at least one of said plurality of threads is implemented using a processor embedded within said programmable logic device (Davis et al., Fig. 4, col. 6, ll. 34-45).

Claim 14, Davis et al. disclose the method of claim 1, wherein said step of defining said first attributes comprises:

including a function block to implement a thread of said plurality of threads (col. 8, lines 39-44; col. 9, lines 5-34; Figs. 10-13; col. 10, lines 30-40).

Claim 15, Davis et al. disclose the method of claim 1, wherein said step of defining said first attributes comprises:

defining an instruction set for a thread of said plurality of threads ("hardware objects"), said instruction set defining communication with an interface logic block (col. 3, ll.25-31; Figs. 5-6, col. 6, ll. 46 to col. 7, ll. 30).

Claim 16, Davis et al. disclose the method of claim 1, further comprising at least one of:

defining fifth attributes for signal groups within said message processing system (Figs. 21-23; col. 16. ll. 55 to col. 17, ll. 9);

defining sixth attributes for run-time reconfiguration of said integrated circuit (abstract; Fig. 27; col. 19, ll. 4-21);

defining seventh attributes for implementation metrics associated with said message processing system (abstract, Fig. 6, col. 6, ll. 55-67); and

defining eighth attributes for debugging information for said message processing system (col. 2, ll. 38-49).

Claim 17 and similarly recited claim 24, Davis et al. disclose a method (claim 17) /computer readable medium (claim 24) of providing a programming interface for a design tool, said design tool adapted to implementing a message processing system using an integrated circuit, the method/computer medium comprising:

providing a first set of primitives (Figs. 5-6, col. col. 6, lines 55 to col. 7, ll. 12, Davis et al. disclose an Atomic Object comprised of logic elements (" a set of primitives")) to specify attributes for a plurality of threads (Davis et al. , col. 3, lines 25-30 see "hardware objects"; Fig. 9-10, col. 8, line 39 to col. 9, line 38);

providing a second set of primitives (Figs. 5-6, col. col. 6, lines 55 to col. 7, ll. 12, Davis et al. disclose an Atomic Object comprised of logic elements (" a set of primitives")) to specify attributes for a memory associated with said integrated circuit (col. 3, lines 25-30 ; col.9, lines 17-24);

providing a third set of primitives (Figs. 5-6, col. col. 6, lines 55 to col. 7, ll. 12, Davis et al. disclose an Atomic Object comprised of logic elements (" a set of primitives")) to specify an interconnection topology associated with at least one of said memory and said plurality of threads (col. 3, lines 25-30 ; col. 17, lines 1-9, see " a direct connection"; col. 9, lines 17-24, see "thread" and "hardware object"); and

providing a fourth set of primitives (Figs. 5-6, col. col. 6, lines 55 to col. 7, ll. 12, Davis et al. disclose an Atomic Object comprised of logic elements (" a set of primitives")) to specify attributes for an interface to at least one of said memory

and said plurality of threads (col. 3, lines 25-30 ; Fig. 5 (element 425), col. 6, lines 46-54; col. 7, lines 16-29 see "the interfaces of the hardware objects").

Claim 18, Davis et al. disclose the method of claim 17, wherein said attributes specified by each of said first, second, third, and fourth primitives comprises at least one of functional attributes and architectural attributes (col.8, lines 39-44; col. 9, lines 17-24; col. 17, lines 1-9; col. 7, lines 16-29).

Claim 19, Davis et al. disclose the method of claim 17, further comprising at least one of:

providing a fifth set of primitives to specify attributes for grouping signals within said message processing system (Figs. 21-23; col. 16. ll. 55 to col. 17, ll. 9);

providing a sixth set of primitives to specify attributes for run-time reconfiguration of said integrated circuit (abstract; Fig. 27; col. 19, ll. 4-21);

providing a seventh set of primitives to specify attributes for implementation metrics for said message processing system (abstract, Fig. 6, col. 6, ll. 55-67); and

providing an eighth set of primitives to specify attributes for debugging information associated with said message processing system (col. 2, ll. 38-49).

Claim 20, Davis et al. disclose the method of claim 17, wherein said first, second, third, and fourth sets of primitives comprise program code for driving said design tool (Figs. 14 and 21-24; col. 9, lines 5-16; col. 16, line 55 to col. 17, line 17).

Claim 21, Davis et al. disclose the method of claim 20, wherein said program code is callable by a second design tool (col. 9, lines 39-53; col. 3, lines 25-31).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 6-7 and 22-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. (US Patent No. 6,230,307) in view of Davidson et al. (US patent No. 6,671,869).

Claim 6 and similarly recited claim 22, Davis et al. substantially disclose the method of claims 6 and 22 respectively, *except* wherein said primitives comprise descriptions configured for interpretation by said design tool.

Davidson et al. disclose a GPI design tool creates and stores the library files (descriptions) in extensible markup language (XML) format (i.e. interpretive language) (col. 13, ll. 9-16).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Davis et al. with the method disclosed by Davidson et al. because such modification including XML descriptions (interpretive language) would facilitate the programming of programmable circuits (col. 10-16).

Claim 7 and similarly recited claim 23, the method of claim 6 and claim 22 respectively, wherein said descriptions comprise extensible markup language (XML) descriptions (Davidson et al., col. 13, ll. 9-16).

8. **Claims 10 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. (US Patent No. 6,230,307) in view of Vandeweerd (US Pub. No. 2004/0006584).

Claim 10, Davis et al. substantially disclose the method of claim 10, *except* wherein each of said plurality of threads comprises a state machine, and wherein said instruction set of each of said plurality of threads is associated with states of said state machine.

Vandeweerd disclose wherein each of said plurality of threads comprises a state machine (paragraphs 0016-0018), and wherein said instruction set of each of said plurality of threads is associated with states of said state machine (paragraphs 0015-0018 and 0094; Figs. 34-37; paragraphs 0481-0521).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of Davis et al. with the method of Vandeweerd because a state machine can be included in a thread model in order to provide a new architecture that is a convenient target for mapping multithread descriptions (Vandeweerd, paragraphs 0048 to 0052).

Claim 12, Davis et al. substantially disclose the method of claim 12 *except* wherein at least one of said plurality of threads comprises a state machine circuit.

Vandeweerd disclose the above-mentioned limitation (paragraphs 0015-0018, 0055-0056; Figs. 34-37; paragraphs 0481-0521).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of Davis et al. with the method of Vandeweerd because a state machine circuit can be included in a thread model in order to provide a new architecture that is a convenient target for mapping multithread descriptions (Vandeweerd, paragraphs 0048 to 0052).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To
Patent examiner
AU 2825

PAUL DINH
PRIMARY EXAMINER